values via the following simple integer approximation to the standard NTSC luminance conversion formula:

Pixel Value=(*R*>>2)+(*R*>>4)+(*G*>>1)+(*G*>>4)+(*B*>>3)

[0135] Please note that unlike in the Color Anti-aliasing mode, the Monochrome Luminance function works solely on the color fields of the current pixel. As a result, the on-chip 2-line ring buffer is not used in this mode.

[0136] Implementation Warning: The simplified math given above is used for ease of understanding, not to convey the actual implementation.

Bit **8**: Scan Line Interrupt Enable

[0137] Setting this bit to 1 enables the output of the secondary display controller **106** Scan Line Interrupt to be generated during the video scan line that is programmed into the Scan Line Interrupt Value register. This interrupt becomes active at the start of the programmed scan line, and remains active for one scan line duration in each frame. This sequence continues as long as the Scan Line Interrupt Enable bit is 1.

Bits **9-11**: Dot Clock Divider

[0138] In order to support minimum power drain, secondary display controller **106** supports the ability to reduce the frequency of the panel interface Dot Clock. The value in this field specifies the crystal oscillator divisor minus one, to yield the system Dot Clock frequency—all video timings are derived from the Dot Clock. If this field contains 0, the Dot Clock is equal to the clock frequency of the crystal, whereas a value of 7 yields a Dot Clock of one-eighth the crystal frequency. Using 4×, the 14.31818 MHz crystal, with nominal programmed video timing parameters that yield a 50 Hz panel refresh rate, and varying the Dot Clock divider alone, results in actual panel refresh rates of 50.00 Hz, 25.00 Hz, 16.67 Hz, 12.50 Hz, 10.00 Hz, 8.33 Hz, 7.14 Hz, or 6.25 Hz.

Bit **12-13**: Reserved

These Read-only bits are reserved.

Bit **14**: Debug Mode Enable

[0139] When the Debug Mode bit is written high, two actions occur. First, the LCD panel interface changes to support a conventional color LCD with color subpixels. Second, SDRAM interface port **220** changes to support 4 MB of SDRAM. On the production of secondary display controller **106** ASICs, this bit should remain cleared to 0.

Bit **15**: Self-Test Mode

[0140] At power-up, secondary display controller **106** samples the BIST pin to determine whether it should enter normal operation—BIST Low or self-test operation—BIST High. The state of the BIST pin is copied to the Self-test Mode bit on exiting reset. Software may also initiate entry into the BIST Mode by writing this bit with a 1, and can restore normal operation by writing this bit with a 0. When secondary display controller **106** is placed in the Self-test Mode, and no input video clock has been detected, secondary display controller **106** automatically cycles its display outputs through the sequences white, black, red, green and blue every two seconds.

Register **2**: Horizontal Resolution

[0141] This 16-bit register contains the number of displayed pixels per horizontal line, which is normally 1200. Please note that due to timing constraints in primary display controller **104**. secondary display controller **106** may receive more input pixel clocks than the number programmed in this register. When this occurs, subsequent clocks, beyond the number of pixels programmed in this register, should be ignored until the next HSync pulse has occurred. Consequently, the number programmed in this register should match the memory pitch, after pixel packing, from one line to the next, as stored in frame buffer **206**

Register **3**: Horizontal Total

[0142] This 16-bit register contains the total number of dot clocks per horizontal scan line.

Register **4**: Horizontal Sync Start and Width

[0143] This 16-bit register contains two 8-bit registers. The most significant byte of the register contains the Horizontal Sync Start register. After "Horizontal Resolution", dot clocks occur on each line. HSync is generated after "HSync Start" additional clocks have occurred. The least significant byte in this register contains the number of clocks so that HSync remains active once HSync has been generated.

Register **5**: Vertical Resolution

[0144] This 16-bit register contains the total number of lines to be displayed per video frame. This normally contains the value 900.

Register **6**: Vertical Total

[0145] This 16-bit register contains the total number of scan-line durations that occur per video frame. For clarity, the TFT panel refresh rate in Hz is equal to the value in the register.

Dot Clock/(Horizontal Total*Vertical Total)

Register **7**: Vertical Sync Start and Width

[0146] This 16-bit register contains two 8-bit registers. The most significant byte in the register contains the vertical sync start register. After Vertical Resolution lines are displayed, VSync is generated after "VSync Start" additional number of times the scan-line has occurred. The least significant byte in this register contains the number of scan lines that VSync should remain active, once VSync has been generated.

Register **8**: Display Timeout Value

[0147] In order to save power, secondary display controller **106** has the capability of automatically powering down the display outputs and entering the secondary display controller **106** Sleep Mode. This register contains the number of output video frames before automatic power down occurs.

Register **9**: Scan Line Interrupt Value

[0148] In order to synchronize processor **102** video output with secondary display controller **106** video output properly, secondary display controller **106** has the ability to enable systems software to synchronize with the display process by generating a processor **102** interrupt at any given line of the